



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sheu, et al. Docket No.: TSM03-0140  
Serial No.: 10/619,828 Art Unit: 2811  
Filed: July 15, 2003 Examiner: TBD  
For: Self-Aligned MOSFET having an Oxide Region below the Channel

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Information Disclosure Statement (1 page)  
IDS Forms PTO/SB/08a and 08b (3 pages) citing (41) references  
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Respectfully submitted,

*Natalie Swider*

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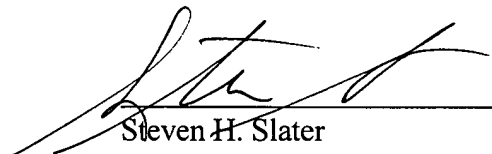
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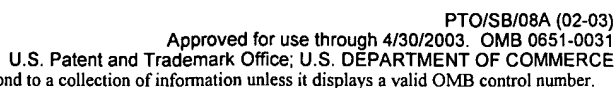
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Respectfully submitted,

25 MAR 2004  
Date

  
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Substitute for form 1449B/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				Application Number	10/619,828
				Filing Date	07/15/2003
				First Named Inventor	Sheu, et al.
				Group Art Unit	2811
				Examiner Name	TBD
Sheet	2	of	3	Attorney Docket Number	TSM03-0140

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	18	ISMAIL, K, <i>et al.</i> , "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.	
	19	NAYAK, D.K., <i>et al.</i> , "Enhancement-Mode Quantum-Well Ge <sub>x</sub> Si <sub>1-x</sub> PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.	
	20	GAMIZ, F., <i>et al.</i> , "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.	
	21	GAMIZ, F., <i>et al.</i> , "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, (July 1, 2002), pp. 288-295.	
	22	MIZUNO, T., <i>et al.</i> , "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp.7-14.	
	23	TEZUKA, T., <i>et al.</i> , "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, (2002), pp. 96-97.	
	24	JURCZAK, M., <i>et al.</i> , "Silicon-on-Nothing (SON) - an Innovative Process for Advanced CMOS," IEEE Transactions on Electron Devices, Vol. 47, No. 11, (November 2000), pp. 2179-2187.	
	25	JURCZAK, M., <i>et al.</i> , "SON (Silicon on Nothing) - A NEW DEVICE ARCHITECTURE FOR THE ULSI ERA," Symposium on VLSI Technology Digest of Technical Papers, (1999), pp.29-30.	
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	27	TIWARI, S., <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, (1997), pp.939-941.	
	28	OOTSUKA, F., <i>et al.</i> , "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meeting, (2000), pp. 575-578.	
	29	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers - I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, (1974), pp. 118-125.	
	30	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers - II. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks," Journal of Crystal Growth, Vol. 29, (1975), pp. 273-280.	
Examiner Signature			Date Considered

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Sheet	3	of	3		

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	31	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers - III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	32	SCHÜPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
	33	MATTHEWS, J.W., "Defects Associated with the Accommodation of Misfit Between Crystals," J. Vac. Sci. Technol., Vol. 12, No. 1 (Jan./Feb. 1975), pp. 126-133.	
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	36	SHIMIZU, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.	
	37	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.	
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	39	YANG, F.L., et al., "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, 2002, pp. 104-105.	
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	41	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.	
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